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# Performance and Design of a Reduced Complexity Iterative Equalizer for Precoded ISI Channels

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**Abstract**— This paper considers the performance and design of a reduced complexity iterative equalizer, for a system including a rate one recursive channel precoder. Recursive channel precoders have been shown to yield significant performance gains, in wireless communication systems, if designed correctly. Extrinsic information transfer (EXIT) charts are used to predict system performance and as a configuration design tool, to determine powerful precoder and detector parameters. Bit error rate (BER) results for BPSK and 8-PSK modulation are presented, to verify the performance predictions of the EXIT chart analysis. Results show that even with large degrees of state reduction, the iterative receiver can achieve significant interleaver gain, associated with the inclusion of the recursive precoder.

## I. INTRODUCTION

Communication systems that transmit data over channels that suffer from inter-symbol interference (ISI) must employ some form of ISI mitigation technique at the receiver. This is necessary to protect the integrity of the transmitted data and to ensure a high quality of service to higher network layers. One method of achieving this robustness is to employ an iterative receiver architecture as described in [1]. To enable iterative reception, redundancy is added at the transmitter via a forward error correcting code (FEC). When the code is separated from the channel by an interleaver, the concatenation it forms with the ISI channel is considered analogous to a serial concatenated code. As such, it can be detected in a turbo fashion similar to that described in [2].

When the channel is non-recursive, which is the case for all wireless channels, then the gain of the iterative receiver is limited since there is no interleaver gain due to the ISI channel. In this case, the performance of the outer FEC code in additive white Gaussian noise (AWGN) represents a bound on receiver performance. In order to achieve performance better than this, either the outer code can be replaced with a turbo code, as suggested in [3], or the channel can be made to appear recursive to the receiver, thus enabling interleaver gain. The latter technique, which has been investigated in depth for magnetic recording channels, employing high rate codes for partial response channels [4] and for general ISI channels by [5], [6], is very appealing for two main reasons. Firstly, because the recursive precoder is rate one, it introduces no additional coding rate overhead and secondly, under certain conditions, it introduces no additional complexity at the receiver. This feature is very attractive because the major drawback of

iterative equalization with turbo detection, developed by [3], is very high receiver complexity.

The work of [5] and [6] for general ISI channels, considers precoding only for binary modulation schemes. In order to achieve high data rates in a limited bandwidth, higher modulation orders must be employed. In [7] a binary precoder for 8-PSK modulation was considered and its performance presented. With the use of modulation orders greater than two, the complexity of a maximum a-posteriori (MAP) channel detector using the BCJR algorithm [8] becomes prohibitive. This is especially true for ISI channels exhibiting large excess delay. Reduced complexity versions of the BCJR algorithm, for use in iterative receivers, based on the T and M algorithms [9] and reduced state sequence estimation (RSSE [10]) [11] have been presented for non-recursive channels. In this paper, the performance and design of an iterative receiver based upon a reduced state soft input soft output (RS-SISO) detector is analysed for BPSK and 8-PSK modulation over precoded recursive channels.

In the next sections, the transmit chain including the channel precoder and the iterative receiver are described. EXIT charts, developed by [12] and employed by [13] for iterative equalizers, are used in conjunction with BER performance simulations to analyze various combinations of precoder and RS-SISO parameters, for both BPSK and 8-PSK modulation.

## II. SYSTEM MODEL

The transmission system depicted in figure 1 is considered in this paper. The outer FEC encoder, which has memory  $m_F$ , accepts blocks of length  $K$  binary data bits, which are encoded to form a sequence  $\mathbf{c}$ , containing  $N$  encoded bits, which includes tail bits for proper trellis termination. The rate of the outer code is given by  $R_F = K/N$ . The encoded bits are bitwise interleaved, with a random interleaver of size  $N$ , denoted in figure 1 by the  $\Pi$  symbol. The output of the interleaver  $\mathbf{y}_n = [\mathbf{y}_0, \mathbf{y}_1, \dots, \mathbf{y}_{K-1}]$  is a length  $S \times Q$  sequence, partitioned into  $S$  symbols, each containing  $Q$  bits. The dimension  $Q$  is particular to the modulation scheme under consideration. The rate one binary precoder codes the sequence  $\mathbf{y}_n$  to form the recursive sequence  $\mathbf{p}_n$ , also containing  $S \times Q$  bits. This precoding is described in detail in section III. The M-ary symbol mapper, maps each  $\mathbf{p}_n$  to a Gray coded symbol  $x_n$  from the  $2^Q$ -ary symbol alphabet  $\lambda_i$ , defined for each

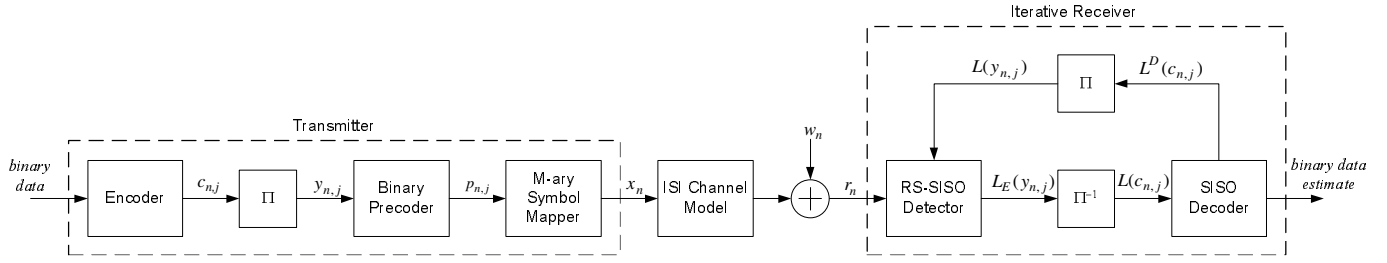


Fig. 1. System model block diagram, showing the binary precoder in the transmitter and an iterative receiver

modulation scheme. The symbol alphabets for BPSK and 8-PSK modulation are taken from [14].

Transmission is considered over a discrete time equivalent channel model (DTECM), where the effects of transmit filtering, the radio propagation channel and receive filtering are concatenated and sampled at the symbol rate [14]. The channel model takes the form of a linear filter with  $L$  time varying coefficients  $\mathbf{h}(t) = [h_0, h_1, \dots, h_{L-1}]$ . The receiver therefore observes a sequence of symbols  $r_n$  given by

$$r_n = \left( \sum_{k=0}^{L-1} h_k x_{n-k} \right) + w_n. \quad (1)$$

The noise samples  $w_n$  are assumed to be Gaussian and white and have noise variance  $\sigma_w^2$ , under the assumption that the receive filter is an optimum whitening matched filter.

An iterative equalizer, which functions in the manner described in [1] is employed at the receiver. The SISO detector accepts as its inputs, the received sequence  $\mathbf{r}$ , a channel estimate  $\hat{\mathbf{h}}$  and a-priori log likelihood ratios (LLR's)  $L(\mathbf{y}) = [L(y_0), L(y_1), \dots, L(y_{N-1})]$ , which in the first instance are all zero to reflect the lack of any a-priori information about the transmitted symbols. It outputs the extrinsic LLR's  $L_E(y_{n,j}) = L(y_{n,j}|\mathbf{r}) - L(y_{n,j})$  about the interleaved encoded bits. The a-posteriori LLR  $L(y_{n,j}|\mathbf{r})$  is calculated in a MAP estimator as:

$$L(y_{n,j}|\mathbf{r}) = \ln \left[ \frac{\sum_{\mathbf{y}: y_{n,j}=1} p(\mathbf{r}|\mathbf{y})P(\mathbf{y})}{\sum_{\mathbf{y}: y_{n,j}=0} p(\mathbf{r}|\mathbf{y})P(\mathbf{y})} \right]. \quad (2)$$

The reduced state Max-Log-MAP detector used in this paper to calculate an approximation to equation 2 is described in section IV. The only input to the decoder  $L(c_{n,j})$  is a deinterleaved version of  $L_E(y_{n,j})$ , no separate a-priori information is available to the decoder. The decoder outputs extrinsic LLR's  $L_D(c_{n,j})$ , which when interleaved can be used as a-priori information for the detector. This iterative process continues until a predetermined stopping criterion, such as a fixed number of iterations is achieved. At this point, hard decisions are made at the output of the decoder, forming an estimate of the input binary data stream.

### III. BINARY RATE ONE RECURSIVE PRECODING FOR BINARY AND NON-BINARY MODULATION

The binary precoder shown in figure 1 transforms the input vector  $\mathbf{y}_n$  containing  $Q$  bits to the vector  $\mathbf{p}_n$  also containing

$Q$  bits, according to the state of the precoder. The precoder may be described in terms of a feedback polynomial for a recursive encoder, as in [5], however when  $Q > 1$  this becomes unwieldy. A simpler approach uses discrete time state-space equations [7]. A generic precoder, with order  $m_P$  and  $S_P = 2^{m_P}$  states, can be described by the following equations

$$\mathbf{s}_{n+1} = \mathbf{s}_n \mathbf{A} + \mathbf{y}_n \mathbf{B} \quad (3)$$

$$\mathbf{p}_n = \mathbf{s}_n \mathbf{C} + \mathbf{y}_n \mathbf{D}, \quad (4)$$

where  $\mathbf{s}_n = [s_0, s_1, \dots, s_{m_P-1}]$  is the state of the precoder. The dimensions of  $\mathbf{A}$ ,  $\mathbf{B}$ ,  $\mathbf{C}$  and  $\mathbf{D}$  are  $m_P \times m_P$ ,  $q \times m_P$ ,  $m_P \times q$  and  $q \times q$  respectively. In this paper, only a subset of the possible precoders that can be realised for each modulation scheme are considered. If the precode is to be decoded as part of the channel detection process, without increasing the number of states in the RS-SISO detector, relative to the non-precoded case, then  $m_P < L$  must be observed.

### IV. REDUCED STATE MAX-LOG-MAP DETECTOR

The RS-SISO detector is based upon the Max-Log-MAP algorithm described in [15]. The complexity of the detector is further reduced, by applying set-partitioning as described by [10] to produce a reduced trellis for the recursive channel. On the forward recursion of the Max-Log-MAP algorithm a survivor map as described in [11] is produced. This survivor map is used on the backwards recursion in order to determine the bits  $\mathbf{y}_n$  corresponding to a given trellis transition.

### V. EXIT CHART ANALYSIS

EXIT charts are an analysis tool that may be used to predict the convergence and BER evolution of an iterative decoding algorithm. They were developed by [12] and have subsequently been used extensively to examine the performance of iterative algorithms for decoding of for example concatenated codes, iterative equalization and iterative space-time codes. They make it possible to predict the performance of a decoding algorithm by examining the transfer function of each of the receiver component devices independently.

The transfer function,  $T$ , of each device is measured in terms of the transfer of mutual information between the input,  $I_i$ , and output,  $I_o$ , of the device under scrutiny. For the detector the transfer function is defined as  $I_o^{DET} = T^{DET}(I_i^{DET})$  and similarly for the decoder transfer function,  $T^{DEC}$ . The

TABLE I  
PRECODER STATE-SPACE MATRICES

Code	$m_P$	$S_P$	A	B	C	D
A	1	2	[1]	[1]	[1]	[1]
B	2	4	$\begin{bmatrix} 1 & 1 \\ 1 & 0 \end{bmatrix}$	$\begin{bmatrix} 1 & 0 \end{bmatrix}$	$\begin{bmatrix} 1 \\ 1 \end{bmatrix}$	[1]
C	3	8	$\begin{bmatrix} 1 & 1 & 0 \\ 0 & 0 & 1 \\ 1 & 0 & 0 \end{bmatrix}$	$\begin{bmatrix} 1 & 1 & 0 \\ 0 & 0 & 1 \\ 1 & 0 & 0 \end{bmatrix}$	$\begin{bmatrix} 1 \\ 0 \\ 1 \end{bmatrix}$	[1]
D	3	8	$\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$	$\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$	$\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$	$\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$

area under  $T^{DET}$  is  $A^{DET} = \int_0^1 T^{DET}(i) di$ .  $A^{DEC}$  is the area under  $T^{DEC}$ , which is approximately equal to  $A^{DEC} = 1 - R_F$ , for a MAP decoder. Convergence of the iterative algorithm is determined by the criteria

$$T^{DET}(i) > (T^{DEC})^{-1}(i) \quad (5)$$

for all  $i \in [0, 1 - \epsilon]$  where  $\epsilon$  is small. This also implies  $A^{DET} > 1 - A^{DEC}$  for convergence to occur. This criteria can be used to determine suitable system parameters, by determining  $T^{DET}$  and  $T^{DEC}$  for various configurations. The transfer functions in the following section are obtained using the technique described in [13], for at least  $10^7$  transmitted bits.

## VI. PERFORMANCE AND CONFIGURATION ANALYSIS

The configuration and performance analysis presented in this section is for the time invariant channel impulse given by  $\mathbf{h} = \sqrt{[0.45, 0.25, 0.15, 0.10, 0.05]}$ , which is perfectly known to the receiver. This channel profile was first used in [1] to determine the performance of iterative equalization and has subsequently been used in [3] and in [5] for turbo iterative equalization and precoded iterative equalization respectively. The outer FEC codes are 1/2 rate recursive systematic codes with memory  $m_F$  varying between two and four, with corresponding generator polynomials as defined in [16]. The interleaver size  $N$  is fixed at 2000 bits. This represents a compromise between performance and acceptable latency in the receiver. The precoder matrices, with varying memory  $m_P$ , defined in table I are used to illustrate the design of precoded systems with RS-SISO iterative receivers.

There are two major design issues involved in determining the parameters of a precoded system. It is important to achieve both convergence at low SNR and to minimise the converged BER. Figure 2 illustrates the trade off between the two, when a full-state detector is employed. It shows the detector transfer functions for a receiver, when the transmitter includes no precoder and precoders A-C, with BPSK modulation at 2dB SNR. Also shown, are the transfer functions of outer codes with  $m_F$  equal to 2, 3 and 4. To achieve convergence at low

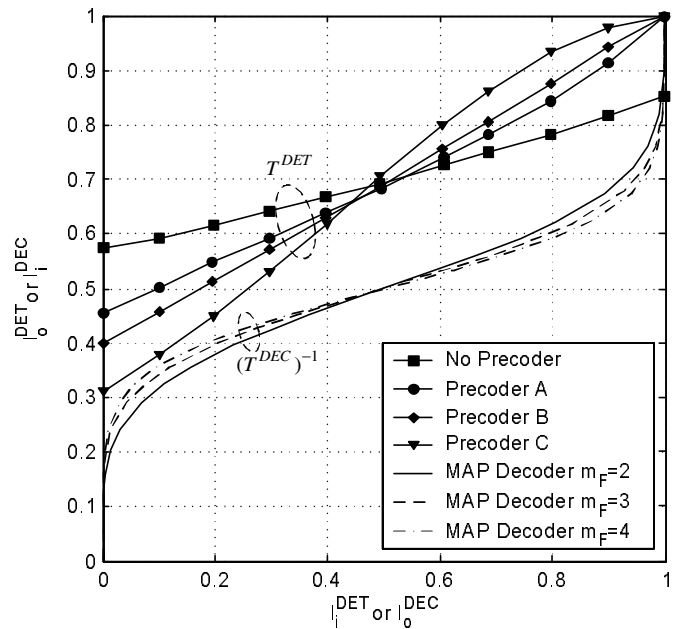


Fig. 2. EXIT charts for a transmitter with no precoder and precoders A-C with BPSK modulation at 2dB SNR, using 16 state a 16 state detector and FEC codes with memory  $m_F = 2 - 4$

SNR, using the criteria in (5), the transfer function of the detector must be maximised for low  $I_i^{DET}$ . The chart shows that the transfer function is maximal for the non-precoded case and decreases as the order of the precoder increases. To aid convergence at low SNR,  $(T^{DEC})^{-1}$  must also be minimised over the same region. This is achieved by minimising the memory of the decoder,  $m_F$ . Throughout the remainder of the paper, the decoder with memory,  $m_F = 2$  is used, to achieve this. To achieve the second design criterion,  $T^{DET}$  should be maximised for high  $I_i^{DET}$ . For the transfer functions shown,  $T^{DET}$  is maximised as the precoder order increases, and is minimal for the non-precoded case. Precoder C, with the highest order, will therefore converge to the smallest BER.

For wireless communication systems, convergence at low SNR is likely to be more important, as a very low BER target is not normally the primary goal, unlike applications in magnetic recoding devices where it is common to seek BER's in the range  $1 \times 10^{-9} \rightarrow 1 \times 10^{-12}$ .

Under the assumption that convergence at low SNR is of primary importance, figure 3 examines the design of a reduced state system without precoding and with precoder A. As the number of states in the RS-SISO detector is reduced, the area under the corresponding transfer function,  $A^{DET}$  is reduced. The area is approximately equal between the non-precoded and precoded case [7] and in this example is 0.72 for the 16-state detector. When the number of states is reduced to 4, in both cases,  $A^{DET}$  reduces to approximately 0.67. Also shown are simulated system trajectories for the 4-state detector. These are obtained by measuring the evolution of mutual information at the input and output of both the detector and decoder as the iterative decoding algorithm is simulated. These trajectories are averaged over the detection of 10000 blocks of data. The trajectories take into account the finite interleaver size and the correlation between the information passed in the iterative process. The trajectories show that the EXIT chart prediction of the transfer of information is very accurate, especially for the first few iterations. Although not shown here due to lack of space, BER's obtained through mapping the mutual information at the output of the decoder,  $I_o^{DEC}$ , using the technique in [13], show good correlation with the BER results shown in figure 4.

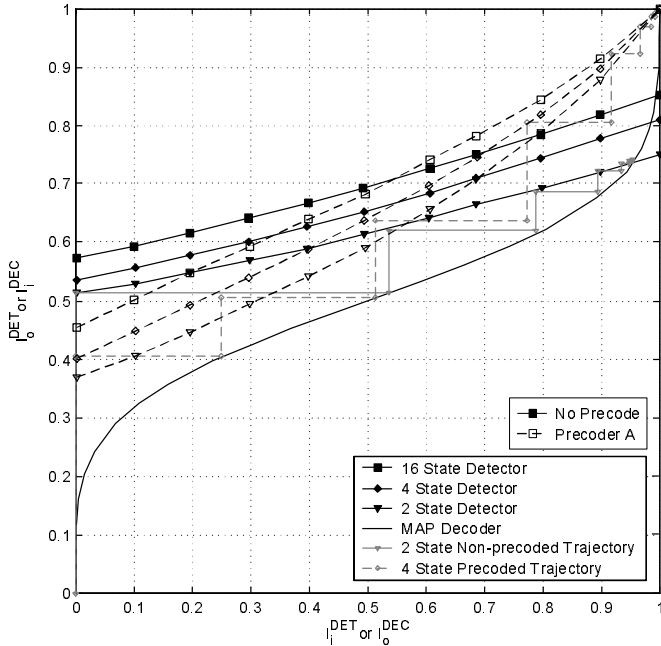


Fig. 3. EXIT charts for a transmitter with no precoder and precoder A, with BPSK modulation at 2dB SNR, including simulated receiver trajectories

Figure 4 shows BER versus SNR for a non-precoded and precoder A system with varying degrees of state reduction in the RS-SISO detector. Examining first the non-precoded sys-

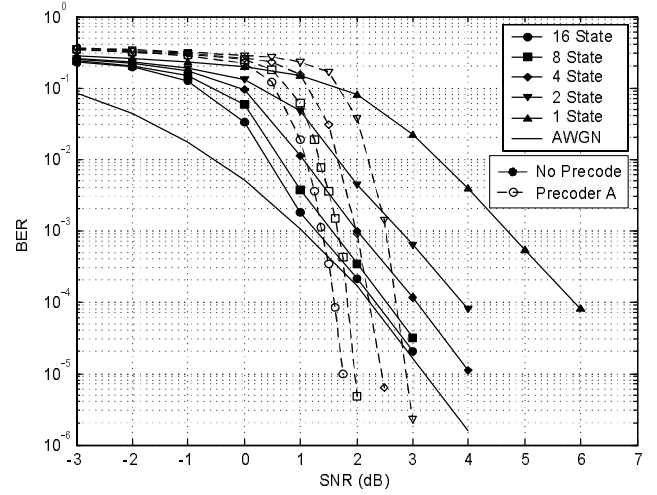


Fig. 4. BER performance with no precoder and precoder A for BPSK modulation, with varying number of states in the detector, after 8 iterations

tem. The full state detector (16-states) achieves performance very close to the bound on performance above 1dB SNR. The curves for the reduced state detector's have the same gradient as the full state detector, but suffer an effective loss in SNR. For example, the 2-state detector has a degradation of 1.6dB at a BER of  $1 \times 10^{-4}$ . This corresponds to the parallel down-shift of the detector transfer function observed in figure 3. The performance of the precoded system is inferior to that of the non-precoded system at low SNR. Above a certain threshold for each detector, the effect of interleaver gain is observed and the precoded system outperforms the non-precoded system. For example, the 2-state precoded system has a 1dB coding gain over the corresponding non-precoded system at a BER of  $1 \times 10^{-4}$ . This system also breaks the bound on performance of the non-precoded system at approximately 2.8dB SNR.

Under the same design assumptions made for BPSK modulation, figure 6 shows the EXIT charts for a RS-SISO detector with varying degrees of state reduction, for a non-precoded system and a system with precoder D, with 8-PSK modulation at 6.0dB SNR. Precoder D has order  $m_P = 3$  which is the minimum required for  $Q = 3$  and therefore should exhibit good convergence at low SNR. Results for other precoders are not presented due to the lack of space. The transfer functions of the detector exhibit the same characteristics as for the BPSK system, due to the application of state reduction. Also shown, are simulated trajectories for the 128-state RS-SISO. For the non-precoded system, the correlation between the EXIT chart and the trajectory is very good. For the precoded system, the correlation is good for the first few iterations, then less accurate.

Figure 6 shows the corresponding BER versus SNR performance with varying degrees of state reduction after 8 iterations. The full state detector would have  $8^4 = 4096$  states. Harsh state reduction has therefore been applied in these results. The non-precoded system only suffers approximately 1.5dB degradation at  $1 \times 10^{-4}$  BER from the bound on

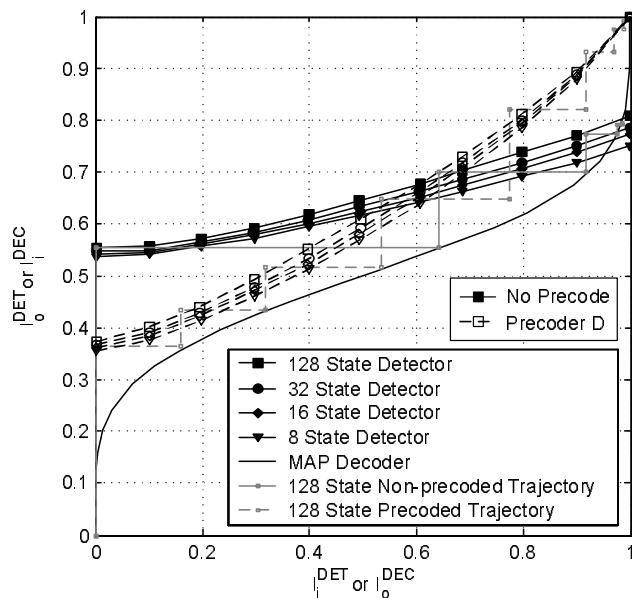


Fig. 5. EXIT charts for a transmitter with no precoder and precoder D, with 8-PSK modulation at 6dB SNR, including simulated receiver trajectories for the 128 state detector

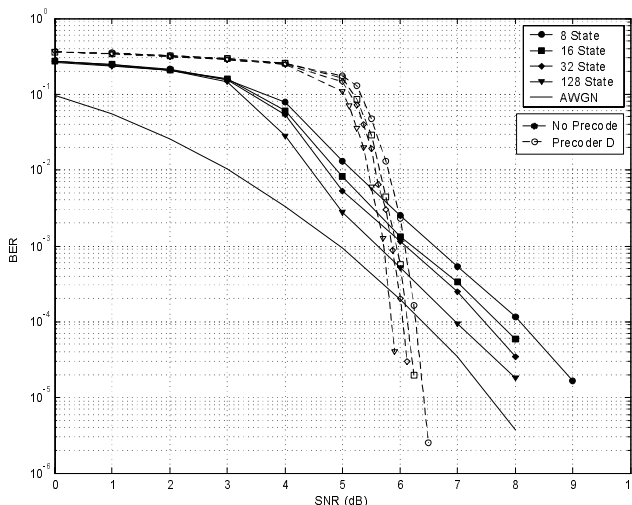


Fig. 6. BER performance with no precoder and with precoder D, for 8-PSK modulation, with varying number of states in the detector, after 8 iterations

performance. The curves for precoder A, show that significant interleaver gain is still achieved even with this state reduction. For the 8-state case, the gain at  $1 \times 10^{-4}$  BER over the corresponding non-precoded case is 1.9dB and is 0.3dB better than the performance bound for the non-precoded system.

## VII. CONCLUSION

The major contribution of this paper is in the analysis of a system that integrates the concepts of rate one recursive binary precoding and RS-SISO iterative equalization. Simulated results demonstrate that the reduced state receiver suffers from a scalable degradation in performance compared to a

full state detector for both a precoded and non-precoded system. The degree of state reduction that is employed is a compromise between performance and acceptable receiver complexity. Results also show that a reduced state receiver can achieve significant interleaver gain when a recursive precoder with appropriate parameters is included in the transmitter. This is true even when large degrees of state reduction have been applied. This is demonstrated by examining an 8-PSK precoded system, where the number of states in the harshest case is reduced by a factor of 512. The paper also demonstrates that EXIT charts are an excellent design and performance analysis tool for reduced state non-precoded and precoded systems. They can be used to determine parameters for the construction of very powerful precoded systems.

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